

Nanostenciling of Functional Materials by Room Temperature Pulsed Laser Deposition

Cristian Victor Cojocaru, Catalin Harnagea, *Member, IEEE*, Alain Pignolet, *Member, IEEE*, and Federico Rosei, *Member, IEEE*

Abstract—We present how various features drawn in a miniature shadow mask (nanostencil) can be efficiently transferred to a surface in the form of three-dimensional nanostructures of metals (Pt, Cr), semiconductors (Ge), and complex oxides (e.g., BaTiO₃) by room temperature pulsed laser deposition. Selective deposition is obtained by interposing a sieve with apertures down to 100 nm between source and substrate. Nanostenciling allows for the organization of structures in predefined architectures with high accuracy. The patterning process is simple and rapid, since it does not imply additional processing steps. It is also parallel, resistless, and does not interfere with the structures' growth dynamics. The material deposited through the stencil mask conserves the desired functionality even at the level of the individual nanostructures. Nanostenciling can be performed in high or ultrahigh vacuum and is suitable for parallel prototyping of fragile or functionalized surfaces.

Index Terms—Atomic force microscopy, functional materials, nanostencils, pulsed laser deposition, unconventional patterning approaches.

I. INTRODUCTION

RESEARCH IN semiconductor physics is continuously motivated by the aim of improving device performance, which usually translates into increasing the density of the integrated components by decreasing their size. Presently nanostructure fabrication is a formidable challenge and the subject of many studies [1]. In this context, top-down and bottom-up fabrication approaches are both extensively explored to tailor nanoscale structures and pattern them in a desired fashion [2].

In top-down fabrication, a “bulk” material is progressively thinned down to obtain ever smaller features (here, by bulk material we mean a continuous thin film). The patterning process is usually achieved by photolithography, the dominant technique employed to manufacture integrated circuits [3]. Modern photolithographic techniques can now define structures as small as 100 nm using ArF and F₂ excimer lasers ($\lambda = 193$ and 157 nm) [4]. Several resolution-enhancement

techniques (RETs) [5] (e.g., phase-shift masks, off-axis illumination, etc.) were recently introduced to achieve even smaller features. Attaining resolution of about 10–20 nm requires the use of smaller wavelengths for mask exposure such as extreme ultraviolet EUV (10–70 nm) or X-rays ($\lambda < 10$ nm). The trend towards device miniaturization has been sustained so far by the constant development of advanced optical lithography for parallel large scale production [6]. For serial, small-scale patterning, electron-beam lithography [7] has been proposed as the technique of choice capable of providing the best feature resolution. This, in turn, increases enormously the costs for surface patterning in the nanometer range.

Unconventional patterning approaches [8] have recently emerged as low-cost, high-resolution alternatives to optical projection lithography. An important approach in this field falls into an area known as “soft lithography” [9]. This is a set of methods that use soft elastomeric stamps, molds and conformable photomasks to pattern two-dimensional (2-D) and three-dimensional (3-D) structures with feature sizes well below 100 nm. Significant advances in defining nanopatterns have been made by nanoimprint lithography (NIL) [10], [11] as well as by its related variant, step and flash imprint lithography (S-FIL) [12] both showing great potential for the semiconductor industry. All these techniques are based on the mechanical transfer of a pattern from the elastomeric stamp or the hard mold to the substrate by direct contact. The common drawback of these alternative solutions, as well as of all lithographic approaches, is that they require resist or polymer processing and, consequently, many chemical, thermal, and etch associated steps. Thus, the ability to fabricate arrays of structures with controlled size and shape, with limited interaction with the substrate of choice and using a minimal number of processing steps, is an ongoing challenge in nanotechnology.

Controlled deposition through a miniature shadow mask (nanostencil) has been revisited and considered as a suitable method to grow patterned nanostructures, in a single deposition step, either in its dynamic or static mode [13], [14]. Most of the work focused so far on metal patterning by evaporation [15]–[22] and lately by pulsed laser deposition (PLD) [23], [24]. More recently, results on organic materials [25] and complex oxide materials [26], [27] were also reported. While offering unlimited freedom in choosing the deposition method, static nanostenciling is in principle applicable to the deposition of arbitrary materials on almost any substrate. It drastically reduces the number of processing operations with respect to resist-based lithography and therefore represents a promising “universal tool” for local deposition of high-resolution and

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The authors are with the INRS—Énergie, Matériaux et Télécommunications, Varennes, QC, Canada (e-mail: rosei@emt.inrs.ca).

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high-purity 3-D nanostructures under high vacuum or ultrahigh vacuum (UHV).

In the following we describe our recent work on the fabrication and patterning of three major classes of materials: metals (e.g., Pt, Cr), semiconductor heterostructures (Ge/Si), and complex ABO_3 -type oxides. We also outline approaches to locally investigate the functionality of the patterned features at the level of individual structures.

II. EXPERIMENTAL

An important goal of our research is to expand the nano-stenciling approach, in its static mode, to different classes of materials and show its unique flexibility for the combination deposited material/substrate. Following this approach, we concentrated on resistless patterning of functional materials by direct PLD through miniature shadow masks with nano-sized apertures drawn in thin microfabricated membranes.

Different types of stencils (in the following, I, II, and III) have been used in our experiments. In principle, for the fabrication of a stencil mask, two main approaches can be applied: the membrane flow process (MFP) and the wafer flow process (WFP) [28]. The first two types of stencils employed in our experiments, (I) laser interference lithography (LIL)-based stencils¹ and (II) DUV-based stencils² were fabricated using the WFP scheme. Membrane etching being the last step, all pattern definition cycles are done on the wafer and performed with typical processing tools for Si microfabrication.

We followed also the MFP for preparing stencils (III) with apertures in the 50–200 nm range by drilling 100–200-nm-thick membranes with a Ga^+ focused ion beam (FIB). Here, a membrane is first formed by lithography and etching processes on the backside of a low-stress silicon-nitride (SiN) coated wafer.³ Then the pattern definition process, in our case FIB milling, takes place directly on the membrane. To reduce charging effects and beam drifting induced during the milling process by the Ga^+ ions, a thin Au/Pd layer (5–10 nm) was initially sputtered on both sides of the membrane.

We conducted the first set of depositions using stencil masks made of ~ 500 -nm-thick silicon nitride nanosieves with circular holes. These stencils have hexagonal arrays of pores (300–500 nm in diameter) patterned and transferred by LIL (I) and anisotropic plasma etching on twelve freestanding, low-stress (LS-SiN) membranes (1 mm in length and 100 μm in width each, 100 μm apart). The membranes are prepared on single crystal Si(100) wafers and the stencil's dimension is $5 \times 5 \text{ mm}^2$ with an active area of $\sim 1 \times 2 \text{ mm}^2$. A second batch of stencils ($1 \times 1 \text{ in}^2$, with 64 processed LS-SiN membranes, 200 nm thick), obtained by DUV lithography (II) [29] was used in a second set of experiments allowing to test the deposition process through features with various sizes (both nm and μm ranges) and shapes.

The miniature shadow masks were mechanically attached and temporarily fixed onto substrates such as Si(100), platinum (Pt) coated silicon, or 0.1%Nb-doped (100)-oriented $SrTiO_3$.

The last two substrates are conductive and can be used as bottom electrodes in further electrical characterization of the material deposited through the nanostencils. The assembly substrate-stencil was mounted in the vacuum chamber of a PLD system, in front of a rotating target.

PLD is a convenient deposition method because of its high versatility in growing stoichiometric thin films [30] on a wide range of substrates. PLD offers the possibility of fine-tuning and controlling deposition parameters (and therefore the properties of the films and structures) such as atmosphere (vacuum or gas), target-substrate distance, laser fluence on target, etc. In particular, the kinetic energy of the ejected atoms can be varied by choosing gas pressure and laser energy.

We used Pt (99%), Cr (99%), and Ge (99%) targets and, for complex oxides, a dense stoichiometric $BaTiO_3$ ceramic. A KrF Lumonics PM-800 excimer laser ($\lambda = 248 \text{ nm}$, pulse duration = 14 ns) was employed for ablation with a 45° incidence angle on the target and a laser fluence between 2 and 4 J/cm^2 . Depositions were carried out in vacuum ($5 \times 10^{-5} \text{ mbar}$) at room temperature, with a laser repetition rate between 5 and 20 Hz. Different sets of thin films (20–200 nm thick) were grown on Si(100) substrates as control specimens and to optimize the growth parameters for each material. The deposition parameters optimized for layers 50–100 nm thick were used to deposit through the stencils. The morphology, structure and composition of the nanostructures were characterized by scanning electron microscopy (SEM), atomic force microscopy (AFM), X-ray diffraction (XRD), and X-ray photoelectron spectroscopy (XPS). AFM measurements were performed in contact mode using Veeco Nanoprobe, general purpose NP cantilevers (Si_3N_4 , tip apex radius 20 nm), and in tapping mode using μ Masch NSC15 cantilevers (Si, radius less than 10 nm). The local ferroelectric properties for the oxides were detected using piezoresponse force microscopy (PFM). PFM tests the piezoelectric and switching properties of ferroelectric materials at the nanoscale, using a modified AFM [31]–[33]. To apply a voltage to the sample, we used conductive cantilevers CSC11B (spring constant 6 N/m) coated with Pt/Ti, from μ Masch. An oscillating testing voltage of 0.5 V was applied between the tip and the conductive substrate on which the structures were deposited. Hysteresis measurements were obtained using an auxiliary digital-to-analog converter of the computer-controlled lock-in amplifier by sweeping the additional dc bias voltage from maximum to minimum values.

III. RESULTS AND DISCUSSION

A. Ordered Metallic Structures

Platinum (Pt) films and structures were grown at room temperature, in vacuum, with a laser fluence set at 4 J/cm^2 and a repetition rate of 20 Hz. Keeping the distance target-substrate at 7 cm, the growth rate achieved was about 0.001 nm/pulse. For preliminary experimental work, we chose stencils with arrays of hexagonal apertures (300–500 nm in diameter). The apertures were replicated on the substrate and ordered arrays of nanostructured Pt were obtained in a single deposition step. AFM analysis performed both in contact and tapping mode showed distinct structures obtained through the whole

¹Stencils fabricated at Aquamarijn Filtration, B.V. The Netherlands.

²Stencils fabricated at EPFL-LMIS1, Lausanne, Switzerland.

³Low-stress SiN membranes purchased from Silson, Northampton, U.K.

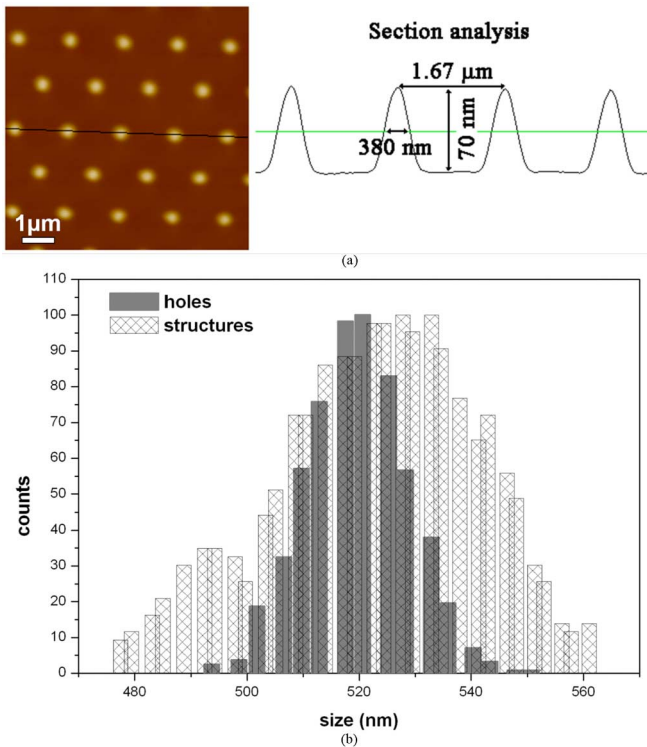


Fig. 1. (a) AFM topography image (recorded in contact mode with Si_3N_4 cantilevers and tip apex radii of 20 nm) and section analysis of Pt structures grown through a sieve with 300-nm-diameter apertures. (b) Pt dot-size distribution (FWHM) after deposition through a stencil with 500-nm aperture diameter.

sieve areas (stripes of $1 \text{ mm} \times 100 \mu\text{m}$). For the sieves with 300-nm-diameter holes, the transfer efficiency was about 80% (e.g., for an 85-nm-thick Pt film the structure heights were about 70 nm) [see Fig. 1(a)]. By varying the number of pulses in PLD, we were able to control the height of the structures in the range 20–75 nm. A broadening of the bottom width of the structures, caused by the shadow effect of the mask, occurs when the stencil is not kept closely enough to the substrate (scattering effect).

Fig. 1(b) reports a histogram with the dots' size distribution after deposition through a 500-nm aperture width sieve. The histogram reveals an average size of 530 nm full-width at height maximum (FWHM). To check the diameter of the holes, we chose randomly an area of one of the sieves, and recorded SEM micrographs, from the membrane's side meant to be in contact with the substrate. After deposition, we also chose randomly a patterned region on the substrate and checked by AFM the lateral size of the replicated structures. The broadening of the structures (right side of the histogram) is due to the shadow effect induced by the gap stencil-substrate. On the other hand, due to inevitable clogging occurring during the deposition, some structures ended up being smaller than the average size (left side of the histogram). A systematic investigation of the shape and size time evolution/degradation of the apertures and structures, including a full statistical analysis, should take into consideration more parameters than what was considered in this limited study, such as the repeatability of all geometrical and physical properties involved during the fabrication process (a more detailed study will be reported elsewhere).

PLD parameters such as distance target-substrate, laser fluence, pressure, as well as the gap between the stencil and the substrate are key parameters that may be tuned during the process to control growth features, e.g., to increase or decrease the aspect ratio of the structures. The gap between sieve and substrate should be as small as possible and uniform over the whole shadowed area. For this purpose a spacer ring about $2 \mu\text{m}$ thick was designed to prevent the masks from touching the substrate in an uncontrolled way, trading off a larger substrate-shadow mask distance against a much better uniformity.

Platinum was initially chosen to prove the feasibility of the combination stencil/PLD. It can then eventually be used, e.g., to prepare templated surfaces that serve as model catalysts for further material growth as suggested in [34], or to fabricate patterned electrodes. However, being a noble metal, platinum is an expensive solution to fabricate patterned electrodes. Thus, we patterned chromium (structures 275–350 nm in lateral size (FWHM) and 15–25 nm in height) following the same approach, reusing the stencils. The process was used to generate patterned top electrodes onto a barium titanate (BaTiO_3) ultrathin film ($\sim 50 \text{ nm}$) previously deposited by PLD. Such “top electrodes” are useful for the local investigation of the films' electrical properties.

A drawback of nanostenciling is the progressive clogging (decrease of the hole size) of the mask's apertures during deposition. A circular hole is estimated to be clogged after evaporating a thickness equivalent up to five times its diameter. However, practice shows that this strongly depends on the deposited material, mask material, and beam collimation [15], [25]. Moreover, certain materials (e.g., gold) can be removed by selective etching. We controlled the PLD process, reusing the stencils (even with different materials) a number of times larger than the value reported above. Thus, the choice of the physical vapor deposition technique used plays an important role and the control of the interaction of the deposited material with the membrane apertures remains a matter of further examination.

B. Controlled Positioning of Germanium Nanostructures

The growth of Ge(Si) on Si surfaces has been the subject of extensive research during the past decade [35]–[37]. SiGe films allow expanding the speed and decreasing the power of integrated devices at relatively low cost. Moreover, light-emitting Ge/Si quantum dot (QD) based devices could expand integrated Si technology to applications in photonics.

By interposing the nanosieve between a Si(100) substrate and the plume generated from a Ge target into the PLD chamber, we achieved direct and controlled Ge structure formation on native-oxide covered Si(100) substrates. Ordered arrays of Ge nanostructures with heights between 12.5 and 40 nm and widths between 200 and 300 nm (FWHM) were obtained just by simple variation of the number of laser pulses on the target. The depositions were performed at room temperature and in vacuum, with stencils previously used for other materials. In the case of PLD, the film thickness adjustment can be realized not only by varying the number of laser pulses but also by changing the distance target-substrate as presented in Fig. 2 where for the same number of 2000 pulses (repetition rate 10 Hz) the distance was increased from 4.5 to 7.5 cm. For different thicknesses of Ge

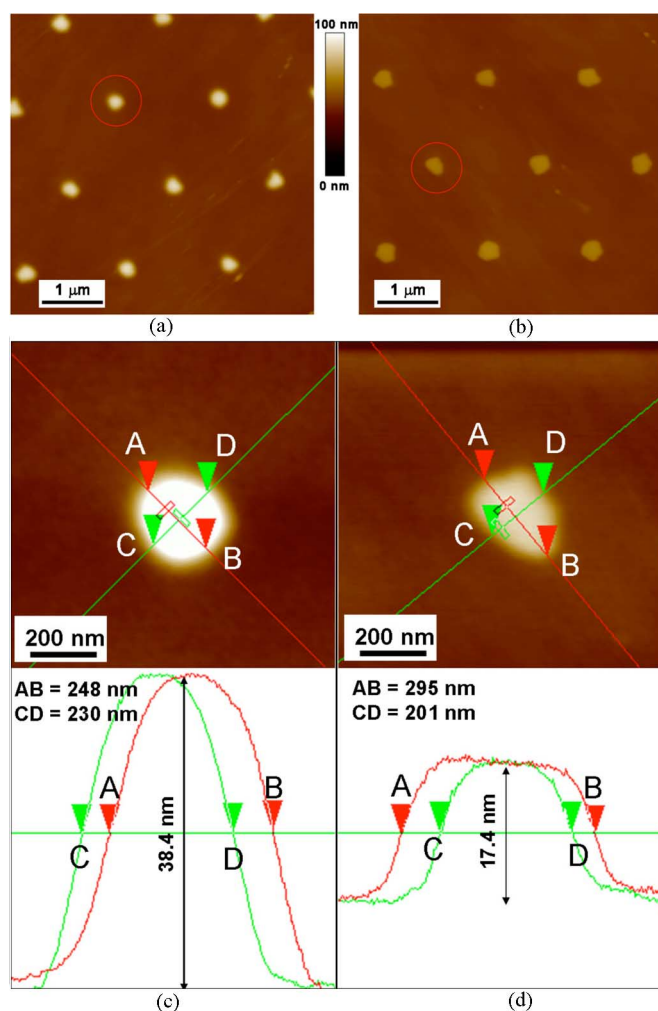


Fig. 2. AFM images of Ge dots on Si(100) patterned at room temperature at two different distances target-substrate for the same number of pulses. (a) and (b) Topography. (c) and (d) Section analysis of an individual structure.

films, the shape of the obtained structures is evolving, from a “dome-like” shape to a faceted “hut-type,” once the thickness of the film decreases, in good agreement with the results recently reported in [38]. The possibility of varying the kinetic energy of the ejected atoms definitely makes the process interesting for the growth of Ge/Si structures and further study is warranted.

X-ray photoelectron spectroscopy for the as-deposited sample was carried out with an Mg $K\alpha$ x-ray source (1253.6 eV). XPS analyses were performed to understand the bonding condition of Ge atoms for both the room-temperature deposited continuous film and the patterned area. The survey spectra shown in Fig. 3(a) clearly illustrate the Ge 3d, 3p, and 3s peaks for the Ge film (80 nm thick) that surrounds the patterned area (Fig. 3(a), top) and the Si 2p and 2s peaks for the patterned area (Fig. 3(a), bottom). The positions of the peaks correspond to typical values found in the literature [39]. The intensity of Ge 3d peak in the spectrum recorded from the patterned area is considerably reduced compared to the one recorded from the film area. That is because the signal originates from a small number of Ge islands covered by an oxide layer, thus less amount of Ge is sampled for the same x-ray spot area of investigation. Considering the universal curve of

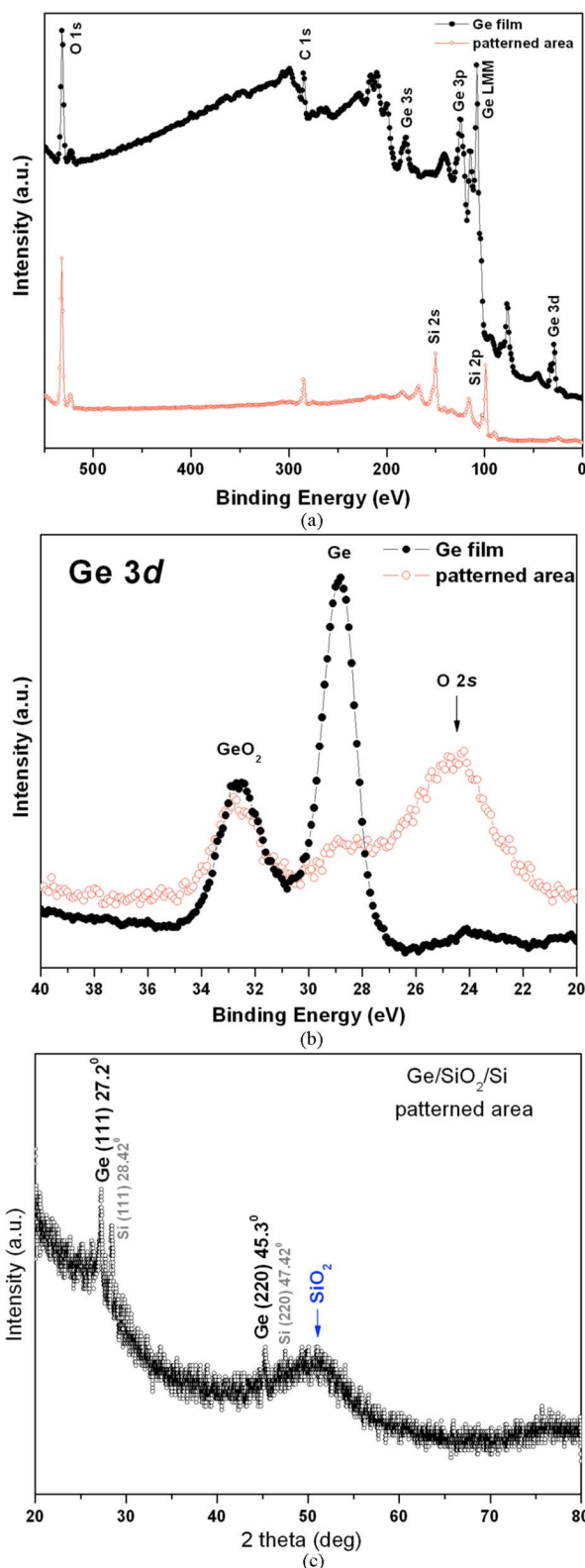


Fig. 3. (a) XPS survey spectra from a continuous Ge film 80 nm thick (graph represented with full circles) and from a Ge/SiO₂/Si patterned area (graph represented with empty circles). (b) Detail of the Ge 3d spectra for a continuous film (full circles) and for a patterned area (empty circles). (c) GIXRD spectra ($\omega = 1^\circ$) for a Ge/SiO₂/Si patterned area after sample annealing at 450 °C for 1 h in an N₂ environment.

photoelectron attenuation depth as a function of kinetic energy [40], for an Mg $K\alpha$ source this should be around 1.5 nm. This represents an upper bound for the oxide thickness since a signal

originating from elemental Ge, within the islands, could still be recorded. No other elements beside Ge, Si, and O were found by XPS, even though the stencils were previously used for depositing other materials, further proving that nanostenciling is suitable to obtain high-purity nanostructures.

To attain a better representation of the contributions Ge–Ge and Ge–O in the 3d peak, we have recorded detailed spectra of this region for both situations [see Fig. 3(b)]. Once normalized, these spectra show similar positions of GeO_2 peaks (32.8 eV patterns and 32.5 eV film) with respect to the Ge peaks (28.9 eV patterns and 28.8 eV film) but a large difference of their intensity ratios. The area ratio of Ge/ GeO_2 was computed and found equal to 1.73 and 0.57 for the measurements on the film and on the patterned surface, respectively. This is not particularly surprising, since for the Ge patterned features the GeO_2 quantity (which in fact is covering entirely the structures) is higher compared to the film, for an identical quantity of Ge. The O 2s peak is also much more intense in the spectrum recorded from the patterned area as there is a strong contribution brought by the presence of the native oxide that covers the Si substrate.

An X-ray diffraction investigation (XRD) was performed after sample annealing at 450 °C in an N_2 environment to investigate the crystallinity of the structures. Even though the amount of Ge is fairly small to perform the usual grazing incidence XRD (GIXRD) measurements, working at grazing incidence with an angle of $\omega = 1^\circ$ and using long times/step for data acquisition, we succeeded in recording an XRD pattern from the patterned area only. As shown in Fig. 3(c), (111) and (220) peaks for Ge are clearly observed along with a broad peak revealing the silicon-oxide layer that is covering the Si substrate. Thus, we were able to reveal the polycrystalline nature of the Ge islands formed after thermal treatment.

We conclude that germanium nanostenciling, combined with any vapor deposition technique such as thermal evaporation, e-beam, or MBE, represents an attractive approach for applications, since it is parallel and does not require resist-based lithography. This is the approach we are currently developing to fabricate QD array architectures of Ge on Si(100) and Si(111) surfaces.

C. Ferroelectric Complex Oxides

To further exemplify the versatility of the nanostencil approach and demonstrate that it can be used to pattern virtually “any material on any substrate,” we used it to grow functional oxide nanostructures. Beyond demonstrating the direct growth of ordered complex oxide nanostructures we were interested in the local characterization of the functional properties of individual structures using PFM. The motivation of this study is to investigate possible size effects (i.e., suppression of ferroelectricity below a critical size at room temperature) in particular on patterned ferroelectric BaTiO_3 nanostructures.

Using type I stencils (circular holes), arrays of BaTiO_3 dot-like structures were grown uniformly through the sieve areas. Nanofeatures could easily be integrated with micrometer features and replicated through the apertures in a sole deposition step, making use of type II stencils which have a collection of assorted features with different shapes and sizes. Fig. 4(a) and

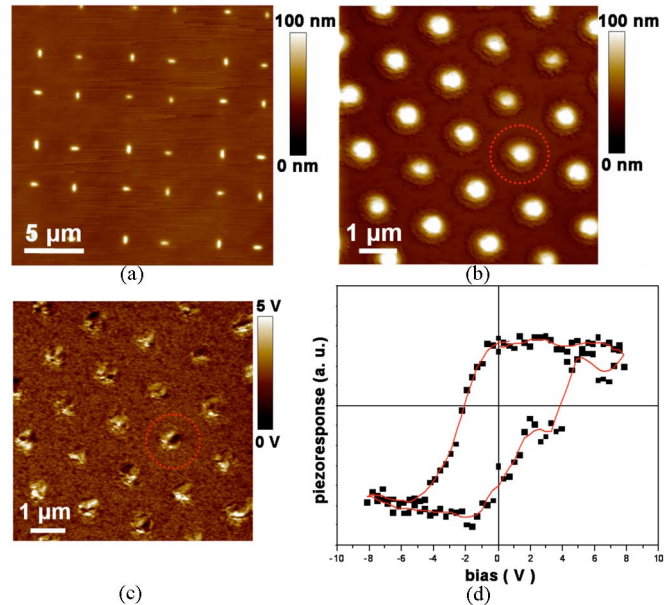


Fig. 4. (a) Contact mode AFM topography of as-deposited BaTiO_3 mesostructures on Si(100) through stencil type II with oblong shaped apertures 200 nm in width and 1 μm in length. (b) AFM topography of 500 nm (FWHM) BaTiO_3 dots on 0.1% Nb-doped SrTiO_3 substrates recorded simultaneously with (c) the piezoresponse domain image. (d) Piezoresponse hysteresis loop obtained from an individual structure.

(b) shows such topography of the ordered structures observed by contact mode AFM.

The “endurance” of the same stencil (originally the holes were 500 nm in diameter) was tested in ten consecutive depositions of a BaTiO_3 layer about 100 nm thick, on different substrates (e.g., Si(100), Pt coated silicon, SrTiO_3 or SrRuO_3). We reused the same stencil even while alternating the target materials: e.g., Cr (two times), PZT (three times), and again BaTiO_3 (two times), at which point structures down to 150 nm (FWHM) are found. Gradually, the sieves suffered structural damages due to repeated mechanical clamping on the substrates and the stencil collapsed before we observed a complete clogging of the holes.

To crystallize the as-deposited BaTiO_3 structures, we used postdeposition annealing in O_2 flow, above 650 °C. GIXRD patterns ($\omega = 1^\circ$) for the patterned structures and surrounding film indicate the presence of a polycrystalline phase very similar to the perovskite cubic phase with grains $\sim 30\text{--}35$ nm in size (estimated with Scherrer’s formula and confirmed by AFM analysis). Polycrystalline fine-grained BaTiO_3 thin films (sizes below 100 nm) exhibit weaker ferroelectric properties than larger grained films/ceramics or bulk single crystals [41]. Yet, we succeeded in recording piezoelectric hysteresis loops from individual structures, thus proving their ferroelectric nature, using long integration times for the lock-in amplifier connected to the AFM via a signal access module.

Fig. 4(b) and (c) present the AFM topography of BaTiO_3 patterned on a 0.1% Nb-doped $\text{SrTiO}_3(100)$ substrate with the piezoresponse domain image simultaneously recorded. The white regions in the z-piezoresponse image reveal that the dots have predominantly a spontaneous polarization oriented “upwards” whereas the dark regions show a spontaneous

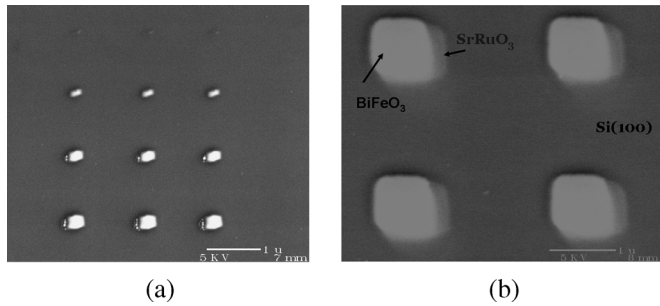


Fig. 5. (a) SEM micrograph of ordered PZT structures (100–300 nm lateral size) deposited at intermediate substrate temperature (400 °C) on Nb-doped SrTiO₃ (100) oriented substrate. (b) Double-level stenciling approach used to create stacked functional structures such as BiFeO₃ on SrRuO₃ on Si (100) by RT-PLD; the shift of the structures is attributed to a slight sliding of the stencil in between the BiFeO₃ and SrRuO₃ depositions.

“downwards” polarization. We attributed the weak PFM signal (the effective piezoelectric coefficient d_{33} was estimated to be 7 pm/V compared to $d_{33} \sim 80\text{--}90$ pm/V in BaTiO₃ single crystal) to the reduced tetragonality of the BaTiO₃ unit cell caused by the fine grain size of the nanostructures (~ 30 nm). Nevertheless, the piezoresponse hysteresis loop [see Fig. 4(d)] reveals that the spontaneous polarization of the patterned BaTiO₃ structures can still be switched and that they retain ferroelectricity.

Lead zirconium titanate (PZT) and multiferroic bismuth ferrite (BiFeO₃) nanostructures have been prepared and patterned using the same RT-PLD shadow masking approach. SEM and AFM analyses showed as in the case of barium titanate well separated and perfectly well-replicated structures with lateral sizes down to 100 nm [see Fig. 5(a)]. Analysis of the out-of-plane piezoresponse images reveal that the structures formed on the substrate (Nb-doped (100)SrTiO₃ in this case) are not epitaxial since z-contrast of all grains does not show only two levels of contrast. Similar to the case of BaTiO₃ structures, after annealing, the structures are formed from grains 20–30 nm in size. A comprehensive study of the effect of the substrate temperature and O₂ background pressure during deposition and furthermore of the postdeposition annealing temperatures on the patterned nanostructures is in progress and will be reported elsewhere [42]. We expect this process to be scalable down to sub-100-nm regime, enabling us to study the size effects on the functional properties of smaller structures.

We have also investigated a multilevel stenciling approach, further extending the versatility of the process, offering a solution for rapid prototyping of functional stacks of materials (such as metal–oxide–metal and/or multiferroic structures) by sequential depositions through the same stencil and without removing it from the substrate in between target changing. For example, controlled deposition of barium titanate or bismuth ferrite on previously patterned strontium ruthenate SrRuO₃ (conductive oxide widely used as bottom electrode in thin film growth processes) may result in lattice-matched nanostructures. As shown in Fig. 5(b), the distance target–substrate, as well as the gap between the stencil and the substrate, must be tuned extremely

well during the deposition process to obtain a perfect overlap of the structures. Ultimately, SrRuO₃ could promote the epitaxial growth of ferroelectric nanostructured BaTiO₃, PZT or BiFeO₃ thus leading to an enhancement of the piezoelectric/ferroelectric properties of the latter. An interesting comparison can be then made between the functional properties of the nanostructures patterned on the “conventional” substrates like Pt coated silicon or conductive Nb-doped SrTiO₃ and on SrRuO₃ structured layers.

IV. CONCLUSION

We have shown how different features drawn in a nanomask can be successfully transferred directly to a substrate in the form of metals, semiconductors, and complex functional oxide nanostructures by PLD. The process is rapid, resistless, and does not interfere with the natural growth dynamics of the structures. This approach conserves the desired functionality of individual nanostructures (proved by PFM measurements for ferroelectric nanostructures). Therefore, nanostenciling is highly flexible, applicable to virtually any kind of material or feature arrangements, and can be performed in high or ultra-high vacuum environment, on any kind of substrate. Further developments of this approach are expected to lead to novel architectures and devices, also providing solutions for critical patterning issues not yet solved.

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Cristian Victor Cojocaru received the Diploma degree in engineering physics from the University of Bucharest, Romania in 1995. He is currently working toward the PhD degree in materials science at INRS—Énergie, Matériaux et Télécommunications, Montréal, QC, Canada.

He was a Physicist Engineer in the NDT laboratory of TMUCB Constanta, Romania. In 2000, he joined the Experimental Dept. II Wafer Bonding group at Max Planck Institut of Microstructures Physics, Halle, Germany, as a Scientific Coworker.

He was involved in the development of wafer bonding and SOI technology for high-temperature electronics and reactive ion etching (RIE) processes. His fields of research interest are micro/nanofabrication, thin-films growth, and unconventional methods for nanoscale fabrication and patterning of functional materials.



Catalin Harnagea (M'04) received the B.Sc. degree in Physics from Alexandru Ioan Cuza University of Iasi, Iasi, Romania, in 1995 and the Ph.D degree from Martin Luther University of Halle, Halle, Germany, in 2001.

From 1997 to 2003, he was with Max Planck Institute of Microstructure Physics (Halle) as a Ph.D student, then Associate Researcher. He studied the properties of ferroelectric thin films and nanostructures by means of voltage-modulated force microscopy. Starting in 2003, he continued his research at INRS-EMT, Montréal, QC, Canada, studying the deposition and the properties of functional nanostructures. He has coauthored 51 peer-reviewed publications (including two book chapters) contributing significantly to the understanding of the local electromechanical measurements on ferroelectric films and the ferroelectric behavior of nanostructures.



Alain Pignolet (M'04) received the Eng.Phys. degree and the Ph.D. degree in physics from École Polytechnique Fédérale de Lausanne (EPFL), Switzerland, in 1986 and 1992, respectively.

Joining the IBM Research Division (T. J. Watson Research Center) as a Postdoctoral Researcher, he began working on high-permittivity relaxor materials, and moved to the Materials Research Laboratory, Penn State University, to continue the research, working mainly with pulsed laser deposition (PLD), reactive multitarget magnetron, and ion-beam sputtering. Returning to Europe in 1994 with a Research Staff Position at Max-Planck-Institut für Mikrostrukturphysik, Halle/Saale, Germany, he set up a laboratory for deposition of ferroelectric thin films using large area PLD. He also worked on the optimization and better understanding of piezo-response force microscopy. Since April 2002, he has been an Associate Professor at the University of Québec's Graduate School INRS—Énergie, Matériaux et Télécommunications, Montréal, Canada, where he is the head of the Ferroic Lab and is working on the deposition and growth of thin films and nanostructures of functional materials, together with their application in microelectronics, nanoelectronics and integrated photonics. He has over 70 publications in the best international journals. He is also coauthor of two book chapters on some aspects of piezoresponse force microscopy, and holds two patents.



Federico Rosei (M'06) received the Laurea degree and the Ph.D. degree in physics from the University of Rome La Sapienza, Rome, Italy, in 1996 and 2001, respectively.

He was a Postdoctoral Research Associate and Marie Curie Fellow at the Center for Atomic Scale Materials Physics, Aarhus, Denmark, from the end of 2000 to April 2002. He then joined the faculty at INRS—Énergie, Matériaux et Télécommunications, University of Québec, Montréal, Canada, as Assistant Professor in May 2002. Two years later, he was promoted to Associate Professor, with tenure. He is recipient of a Strategic FQRNT Fellowship for New Professors from the Province of Québec and holds the Canada Research Chair in Nanostructured Organic and Inorganic Materials. He has coauthored 40 articles in prestigious international journals and has given over 50 invited, keynote, and plenary lectures at international conferences. His research interests focus on the properties of nanostructured materials, and how to control their size, shape, composition, stability, and positioning when grown on suitable substrates. He has extensive experience in fabricating, processing and characterizing inorganic, organic, and biocompatible nanomaterials.