

Tetracene light-emitting transistors on flexible plastic substrates

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(Received 4 August 2004; accepted 22 February 2005; published online 31 March 2005)

We report on organic light-emitting (field-effect) transistors (LETs) fabricated on a flexible and transparent plastic foil (Mylar), acting both as substrate and gate dielectric. The foil is patterned on one side with bottom-contact gold source and drain electrodes, while a thin film of gold is evaporated on the opposite side of the foil to form the gate electrode. A vacuum sublimed tetracene film is employed as an active layer for charge transport and light emission. Atomic force microscopy shows that tetracene films have a good adhesion on Mylar and exhibit a granular structure. The transistor shows unipolar *p*-type behavior with mobilities typically of 5×10^{-4} cm²/V s. Drain-source current and electroluminescence have been simultaneously measured. Provided a suitable gate bias is applied, light emission occurs at drain-source voltages (V_{ds}) above saturation. LETs on plastic substrates could open the way to flexible devices combining the switching function of a transistor and the light emission. © 2005 American Institute of Physics.

[DOI: 10.1063/1.1898429]

Organic semiconductors, based on conjugated small molecules and polymers, offer the opportunity to produce devices on large-area, low-cost, plastic substrates.¹ Research in organic optoelectronics has recently led to the demonstration of colorful thin displays based on organic light-emitting devices (OLEDs).² Organic field-effect transistors (OFETs) are currently under investigation as switches for active matrix-OLED displays.³ Flexible OFETs and OLEDs, based on organic films grown on flexible plastic substrates, have been reported.^{4–7} These findings are attractive as they open the possibility to fabricate active matrix colorful and flexible electroluminescent displays.

Light-emitting (field-effect) transistors (LETs) employing as active layers tetracene films deposited onto SiO₂/*n*-Si have been produced.^{8,9} Recently, the first ambipolar LET has been demonstrated.¹⁰ LETs constitute a class of optoelectronic devices that integrate the switching function of a transistor and the light emission. In principle, with respect to vertically stacked structures typical of LEDs, the presence of the gate electrode in planar LET structures offers remarkable advantages: in the case of ambipolar light-emitting materials,¹⁰ the gate bias would allow to minimize the unbalanced number of holes and electrons in the active layer,¹¹ a crucial topic to obtain high exciton density. Furthermore, the

gate bias would allow to control the location of the exciton recombination region in the transistor channel¹² to minimize exciton quenching at metal electrodes. The device physics of LETs involves multiple processes: light is generated from radiative recombination of excitons formed by holes and electrons injected in the active layer by biased source and drain electrodes, provided a suitable gate bias has been applied. The detailed understanding of these processes and their correlation to the specific device structure of LETs for example in terms of dielectric and electrodic materials and processing, is challenging. In particular, the role played by the dielectric layer in determining the operational device physics is of primary importance. It has been demonstrated that, in organic films-based field-effect devices, charge transport occurs within a thin layer close to the organic/dielectric interface.¹³ The chemical-physical properties of the dielectric surface influence the growth mechanism and morphology of the active layer, which is related to the charge transport, exciton formation, and light emission processes.¹⁴ Moreover, the fabrication process of source and drain electrodes may affect the charge injection mechanism in the organic layer within the transistor channel. The presence of an adhesion layer (typically chromium) between the dielectric SiO₂ and Au electrode, together with possible electrode underetching,⁸ may change the electrode-organic interface responsible for charge injection. Therefore, the investigation of light-

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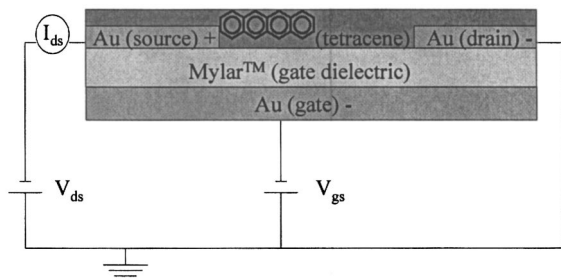


FIG. 1. Structure of the LET device employing a thin Mylar foil as substrate and gate dielectric and a tetracene thin film as active layer.

emitting transistors employing dielectric substrates with different characteristics and gold electrodes fabricated without adhesion layer, provides experimental data useful to shed light onto the working mechanism of the organic LET (OLET) devices.

In this letter we report on the fabrication of LETs based on tetracene films grown on flexible plastic substrates. Tetracene films have been chosen as active materials because of their high hole FET mobility (up to $0.1 \text{ cm}^2/\text{V s}$ ^{15,16}) and their reasonably high fluorescence quantum yield.¹⁷ LETs fabricated on plastic substrates extend the potential of this new class of organic optoelectronic devices opening the way towards all plastic multifunctional field-effect devices.

Figure 1 shows the structure of the device. A 900-nm-thick Mylar™ sheet (DuPont), adapted to an Al frame (not shown in the figure), has been employed as substrate and gate insulator (dielectric constant of 3.3). The Mylar sheet has a dielectric rigidity of 10^6 V/cm that allows to apply gate biases sufficiently high to induce a field effect in the organic semiconductor. The plastic sheet is transparent to ultraviolet and visible light. Bottom-contact Au source and drain electrodes have been patterned on one side of the dielectric using a standard photolithographic technique while the Au gate electrode has been evaporated on the opposite side. Experimental details on the fabrication of the electrical contacts have been reported elsewhere.⁵ Interdigitated electrodes with $W/L=3000$ (W and L are the channel width and length, respectively), with $L=70 \mu\text{m}$, have been used. Prior to organic deposition, the substrates have been rinsed with acetone and isopropyl alcohol and dried in N_2 flux. As a comparison, device structures employing as gate dielectric a 100-nm-thick layer of SiO_2 (thermally grown on $n\text{-Si}$) patterned with bottom-contact Au interdigitated electrodes with $W/L=200$ and $L=5 \mu\text{m}$ have been used. Tetracene (TCI, 98%) has been used as received. Tetracene films with a nominal thickness of 50 nm have been grown by vacuum sublimation at different nominal deposition fluxes, from 0.05 to 5 \AA/s . Atomic force microscopy (AFM) images of films grown on Mylar at 0.1 \AA/s (a) and 5 \AA/s (b) are shown in Fig. 2. The images reveal that tetracene films have a good adhesion on Mylar and exhibit a granular structure. By increasing the deposition flux the grain size decreases whereas the grain shape and size distribution become more regular. Compared to films grown on SiO_2 , at the same deposition flux, films on Mylar have smaller grain size. This can be due to different substrate surface energy or tetracene diffusivity.¹⁶

Drain-source current (I_{ds}) and electroluminescence (EL) measurements have been performed at room temperature under high vacuum (10^{-3} Pa) inside a calibrated integrating

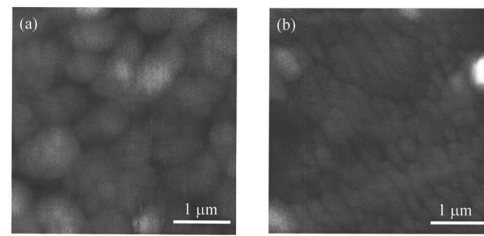


FIG. 2. $4 \times 4 \mu\text{m}^2$ AFM micrographs of tetracene films grown on Mylar having a nominal thickness of 50 nm, grown at nominal deposition fluxes of (a) 0.1 \AA/s and (b) 5 \AA/s .

sphere where high sensitivity light detection has been achieved through a preamplified photomultiplier.¹⁸ A dc power supply (Agilent 6634D) has been used to control the gate-source voltage (V_{gs}) and a source-measure unit (Keithley 236) to control the drain-source voltage (V_{ds}) and to measure I_{ds} (the source electrode being the common ground). In order to avoid aging effects, all measurements have been performed immediately after tetracene film deposition. Figure 3(a) shows the output characteristics of a LET device on Mylar biased as a p -channel FET working in accumulation mode. At a fixed V_{gs} , for low $|V_{ds}|$, $|I_{ds}|$ increases with $|V_{ds}|$ and then attains the saturation ($I_{ds,sat}$) at larger $|V_{ds}|$ ($V_{ds,sat}$). $|I_{ds,sat}|$ increases with the increase of $|V_{gs}|$. Figure 3(b) shows the EL as a function of V_{ds} , corresponding to the I_{ds} reported in Fig. 3(a) (except for the case $V_{gs}=-30 \text{ V}$). For $V_{gs} \leq -70 \text{ V}$, light is emitted by the device. It is clear for the case $V_{gs}=-90 \text{ V}$ that the onset of EL is located at about $V_{ds}=-60 \text{ V}$. At a fixed V_{gs} , EL continuously increases with the increase of $|V_{ds}|$, despite the quasicontant value of I_{ds} . As a comparison, Figs. 3(c) and 3(d) show the output characteristics and the corresponding electroluminescence measured for LETs fabricated onto $\text{SiO}_2/n\text{-Si}$. The onset of EL, for $V_{gs}=-40 \text{ V}$, is located at about $V_{ds}=-13 \text{ V}$, which is below the saturation voltage of the drain current. Figure 4(a) shows the transfer characteristics of the Mylar device at the saturation ($V_{ds}=-90 \text{ V}$). I_{ds} and EL are reported on the left and right y axis, respectively, as a function of V_{gs} . $|I_{ds}|$ and EL both increase with increasing $|V_{gs}|$. As a comparison, Fig. 4(b) shows the transfer characteristics at the saturation ($V_{ds}=-40 \text{ V}$) and the corresponding electroluminescence mea-

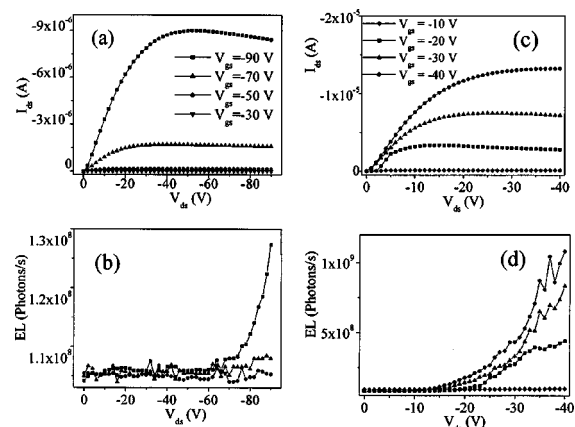


FIG. 3. Output characteristics of tetracene LETs: (a), (b) LET employing a 900-nm-thick foil of Mylar as gate dielectric, $W/L=3000$ and $L=70 \mu\text{m}$; (c), (d) LET employing a 100-nm-thick layer of SiO_2 as gate dielectric, $W/L=200$ and $L=5 \mu\text{m}$. The I_{ds} vs V_{ds} curves are reported in (a), (c) while the corresponding EL vs V_{ds} are shown in (b), (d). Deposition flux of the active layer: 5 \AA/s , nominal thickness: 50 nm.

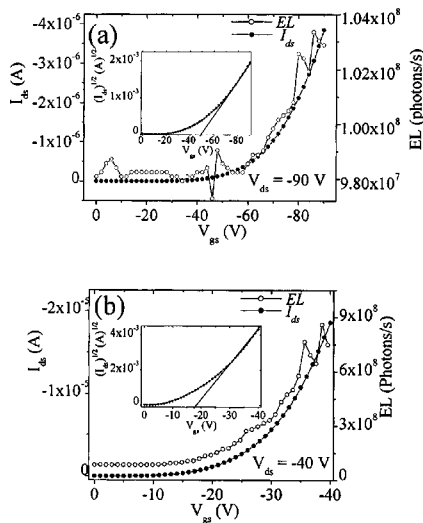


FIG. 4. Transfer characteristics (I_{ds} and corresponding EL vs V_{gs}) at drain current saturation of tetracene LETs employing as gate dielectric a 900-nm-thick foil of Mylar (a) and a 100-nm-thick layer of SiO_2 (b). The insets show the square root of I_{ds} as a function of V_{gs} . Deposition flux of the active layer: 5 Å/s, nominal thickness: 50 nm.

sured for LETs fabricated onto $\text{SiO}_2/n\text{-Si}$. The correlation between transistor current and light emission for tetracene-LETs produced on Mylar is in reasonable agreement with that observed for LETs produced on SiO_2 . This is remarkable in view of the different morphologies observed for the tetracene-films grown on Mylar and on $\text{SiO}_2/n\text{-Si}$.¹⁶ However, the external quantum efficiency (i.e., the number of photons emitted per electrons flowing in the device) of LETs on Mylar is about one order of magnitude lower than on $\text{SiO}_2/n\text{-Si}$. Indeed, in LETs on Mylar, light emission occurs invariably at $|V_{ds}|$ larger than $|V_{ds,sat}|$ while in LETs on $\text{SiO}_2/n\text{-Si}$, for the highest values of $|V_{gs}|$, it occurs already in the linear region of the output curves.^{8,9,16} For LETs on Mylar, this would imply a hole-depleted region next to the drain electrode, where the emission is expected to occur.⁸ This is likely related to the different distributions of the internal electric fields in the two devices. The hole FET mobility (μ) has been calculated in saturation¹⁹ using the following equation:

$$|I_{ds,sat}| = \frac{W}{2L} \mu C_i (V_{gs} - V_T)^2,$$

where C_i is the dielectric capacitance per unit area (3×10^{-9} and 3.5×10^{-8} F cm^{-2} for a 900-nm-thick Mylar foil and a 100-nm-thick SiO_2 layer, respectively) and V_T is the threshold voltage, deduced from the intercept at $y=0$ of the $(|I_{ds,sat}|)^{1/2}$ vs V_{gs} plot (see inset of Fig. 4). The hole FET mobility for LETs on Mylar, calculated on several samples prepared in different deposition runs, is typically 5×10^{-4} $\text{cm}^2/\text{V s}$. The values are lower by about one order of magnitude than those observed for tetracene FETs fabricated on $\text{SiO}_2/n\text{-Si}$ substrates.^{15,16} Moreover, the mobility does not strongly depend on the deposition flux, as in the case of tetracene-LETs on $\text{SiO}_2/n\text{-Si}$.¹⁶ This result points again to the crucial role played by the dielectric in determining the device characteristics. Work is in progress to tailor substrate surface properties by means of functionalization and appropriate surface cleaning. The possible influence of the hole mobility on the onset voltage of EL, as well as the EL inten-

sity and efficiency is under investigation both for tetracene-LETs on $\text{SiO}_2/n\text{-Si}$ and on plastics. Preliminary results indicate that emission takes place in LETs exhibiting mobilities ranging from 1×10^{-4} to 1×10^{-1} $\text{cm}^2/\text{V s}$.^{8,9,16} The comparison between devices fabricated on SiO_2 with underetched electrodes⁸ and devices fabricated with nonunderetched electrodes shows that electron injection from gold to tetracene occurs in both cases. Therefore underetching is not to be considered a necessary condition to explain the injection mechanism.

In summary, we fabricated the first organic LETs on flexible plastic substrates by physical vapor deposition of tetracene films on Au-patterned Mylar foil employed as substrate and gate dielectric. Tetracene films show a good adhesion on Mylar and exhibit a granular structure with a grain size decreasing with increasing deposition flux. The devices behave as p -channel transistors working in accumulation mode. Light emission occurs for drain-source voltages well above the V_{ds} saturation value. This behavior is different from that of LETs fabricated on SiO_2 , which may generate light starting from the linear region. Taking advantage of the ultraviolet and visible transparency of the dielectric sheet, attractive developments of the device structure can be envisaged. Indeed, transparent or semitransparent gate electrode would allow light collection from both sides of the film. Alternatively, a highly reflective metal deposited as gate electrode on one side of the sheet would optimize light extraction from the opposite side.

The authors acknowledge the EU-IST-FET Program under Project Nos. IST-33057 (ILO) and IST-39262 (ARI-ANNE) and the Italian Ministry for Research Program under Project FIRB. Support by Fondazione del Monte di Bologna e Ravenna is kindly acknowledged.

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